REMARKS

Claims 1-48 are pending in the present application.

Claims 1-48 stand rejected under 35 U.S.C. §102(b) as being anticipated by Liencres et al. (U.S. Patent No. 5,434,993) (hereinafter "Liencres"). Applicant respectfully traverses this rejection.

Applicant's claim 1 recites

"A system, comprising:

a plurality of nodes coupled by an inter-node network, wherein each node includes a plurality of active devices, a memory subsystem, and an address network and a data network respectively configured to convey address packets and data packets between the plurality of active devices and the memory subsystem;

wherein a memory subsystem included in a node of the plurality of nodes is configured to maintain a response indication indicating whether the memory subsystem should send a data packet corresponding to a coherency unit in response to receiving from an active device in the node an address packet requesting an access right to the coherency unit;

wherein the node is configured to store a node identifier for the coherency unit, wherein the node identifier identifies a different node of the plurality nodes in which the coherency unit is in a modified global access state." (Emphasis added)

The Examiner asserts Liencres teaches each and every limitation recited in Applicant's claim 1. More particularly, the Examiner asserts Liencres teaches in in FIG. 3a, an internode network as being element 31, an address network coupling the active device the interface and the memory as being element 31. Applicant respectfully disagrees with the Examiner's characterization of Liencres and the application of Liencres to Applicant's claims.

Specifically, as illustrated in Fig.3a and 3b of Liencres, element 33 cannot be the address network as recited in Applicant's claim 1 because it only couples the bus controller 31 to the processor cache controller 35. It does not couple the active device, the interface, and the memory as recited in claim 1. In addition, element 35 is a cache controller, this is not an active device; processor 21 is an active device, and element 32 is the entire cache subsystem, not a memory subsystem.

However, the above notwithstanding, Applicant further asserts Liencres actually teaches at col. 7, lines 7-10

> "The bus cache controller 31 maintains a cache directory 46 containing the address tags and status bits for the data in the cache memory 37." (Emphasis added)

Liencres also discloses at col. 1 lines 61-65

> "To maintain cache consistency, several status bits are usually maintained in the cache directory which reflects the current state of the information in each cache line. Common status bits maintained include a "valid" bit, a "shared" bit, and an "owned" bit." (Emphasis added)

Liencres further discloses at col. 8, lines 12-24

> "when the processor 21 requires data that is not stored in the local cache memory 37, a cache miss occurs. The processor cache controller 35 issues a read request packet containing the required memory address to the bus cache controller 31 through the cache bus 33. As discussed in the read transaction section, the bus cache controller 31 responds to the read request packet by broadcasting a corresponding read request packet across the memory bus 25. The appropriate memory unit or processor subsystem on the memory bus 25 should eventually respond to the read request packet with a read reply packet containing the requested data." (Emphasis added)

Further, Liencres dislcoses in col. 7 "Read transactions"

> "When a memory request by the processor 21 cannot by fulfilled by the data in the processor cache memory 37, the processor cache controller 35 sends a read request packet across the cache bus 33 to the bus cache controller 31. The bus cache controller 31 proceeds to broadcast a corresponding read request packet across the memory bus 25. The read

> transaction initiated by the bus cache controller 31 consists of two packets: a read request packet sent by the bus cache controller 31 on the memory bus 25 and a read reply packet sent by another device on the memory bus. The read request packet contains the address of the memory requested by the processor cache controller 35 and is broadcast to all entities on the memory bus 25. A device on the memory bus 25 that contains the requested memory address responds to the read request packet with a read reply packet containing the subblock which includes the requested memory address. The read reply packet is generally issued by the main memory 23 except when the desired memory address is "owned" by another processor subsystem 20. In that case, the processor subsystem that owns the subblock must generate a read reply packet with the requested data."

From the foregoing disclosure, it appears Liencres is merely stating that the cache controller maintains status bits for each cache line and the status bits are what one would customarily expect (e.g., valid, shared, owned). The status bits do not indicate who the owner is. In addition, Liencres is also disclosing in response to a read request, eventually the owner will respond with the data. Further, in the Read transactions section, Liencres is only teaching that read requests are met with replies that contain the data. However, Applicant cannot find any teaching in Liencres to the interface maintaing an explicit indication indicating whether the reply data should be sent. Applicant asserts it appears Liencres is silent as to how the determination is made. In addition, Applicant cannot find any refenerence in Liencres to a node ID for the coherency unit that identifies the node in which the cherency unit is in a modified state.

Thus, Applicant asserts Liencres does not teach or disclose "each node includes a plurality of active devices, a memory subsystem, and an address network and a data network **respectively** configured to convey address packets and data packets between the plurality of active devices and the memory subsystem;" and "wherein a memory subsystem included in a node of the plurality of nodes is configured to maintain a response indication indicating whether the memory subsystem should send a data packet corresponding to a coherency unit in response to receiving from an active device in the node an address packet requesting an access right to the coherency unit;" and "wherein the node is configured to store a node identifier for the coherency unit, wherein the node

identifier identifies a different node of the plurality nodes in which the coherency unit is in a modified global access state," as recited in claim 1.

Accordingly, Applicant submits claim 1, along with its dependent claims, patentably distinguishes over Liencres for the reasons given above.

Applicant's claim 17 recites features that are similar to the features recited in claim 1. Thus Applicant submits claim 17, along with its dependent claims, patentably distinguishes over Liencres for at least the reasons given above.

Claim 33 recites method comprising in pertinent part

"in response to said receiving, the memory subsystem sending a responsive data packet to the active device dependent on **response indication** associated with the coherency unit;

the node sending a coherency message requesting the access right to a different node of the plurality of nodes in response to **a node identifier identifying the different node** as a node in which the coherency unit is in a modified global access state."

As described above, these features are not taught in Liencres. Accordingly, Applicant submits claim 33, along with its dependent claims, patentably distinguishes over Liencres for the reasons given above.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-13501/SJC.

Respectfully submitted,

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